Staircase Control of Hybrid Multilevel Inverter Topology with Reduced Number of Power Electronic Components

K.Srinivasu, S.M.Shariff, K.Satyanarayana

Abstract: Multilevel inverter execution is high contrasted with the ordinary two level inverters because of their lessened harmonic distortion, lower electromagnetic interference. Then again the fundamental disadvantage of multilevel inverter is expanded number of power electronic switches, complex pulse width modulation control and adjusting of capacitor voltages. In this paper proposes a hybrid single phase inverter topology comprises of littler number segments with low convoluted gate drives and control signals. This paper additionally introduces the most appropriate control and balance strategies like Staircase modulation technique with sinusoidal wave as reference.

In this paper proposed multilevel inverter topology is studied for three distinct levels of yield voltage like 7, 11 and 15. Likewise proposed multilevel inverter is contrasted and right now existing inverter topologies. The whole framework is numerically simulated using MATLAB/SIMULINK and the simulation results are displayed.

Index Terms— Cascaded Multilevel Inverter (CMLI), Pulse Width Modulation (PWM), Staircase Modulation, Switching Frequency, Symmetric & Asymmetric Multilevel Inverter, Total Harmonic Distortion (THD).

1. Introduction

A multilevel inverter (MLI) is a power electronic structure that creates a fancied yield voltage from various levels of dc voltages as data sources. Lately multilevel power transformation has been building up the zone of force hardware rapidly with great potential for further advancements. The remarkable uses of this innovation are in the medium to high voltage ranges. The early presented topology is the arrangement H- bridge outline [2]. This was trailed by the diode-clamped inverter which uses a bank of arrangement capacitors to part the dc transport voltage. The flying-capacitor (or capacitor braced) [3] topology took after diode-clamped following couple of years, rather than arrangement associated capacitors, this topology utilizes gliding capacitors to clasp the voltage levels. Another multilevel outline, marginally unique in relation to the past one, includes parallel association of inverter stages through bury stage reactors [4]. In this plan the semiconductors must square the whole voltage, however share the load current. Likewise, a few combinatorial plans have risen [5], executed falling the major topologies [6–10]; they are called half breed topologies. These outlines can make power quality for a given number of semiconductor gadgets higher than the basic topologies alone because of a duplicating impact of the quantity of levels. Likewise, some delicate exchanging strategies can be actualized for various multilevel inverters to lessen the changing misfortune and to expand productivity. As of late, a few multilevel inverter topologies have been produced.

Shockingly, multilevel inverters have a few weaknesses. One specific disservice is the immense number of power semiconductor switches required. Albeit low voltage rate switches can be used in a multilevel inverter, every switch requires a related gate driver circuits. This may bring about the general framework to be more costly and complex. Along these lines, in reasonable execution, diminishing the quantity of switches and entryway driver circuits is essential.

This paper recommends another topology for cascaded multilevel inverters with a high number of steps connected with a low number of switches and entryway driver circuits for switches. Also, to produce all levels (odd and even) at the yield voltage, three methods for figuring the required dc voltage sources are proposed. At last, the paper incorporates simulation results to demonstrate the possibility of the proposed multilevel inverter.

2. Conventional Cascaded Multilevel Inverters

The full- bridge topology with four switches is utilized to produce a three-level square-wave yield voltage waveform. The cascaded multilevel inverter comprises of arrangement associations of n fullbridge topology. Fig.2.1 demonstrates the arrangement of cascaded multilevel inverter. The general yield voltage of multilevel inverter is given by:

$$V_o=V_{o,1}+V_{o,2}+.....+V_{o,n} \quad (1)$$

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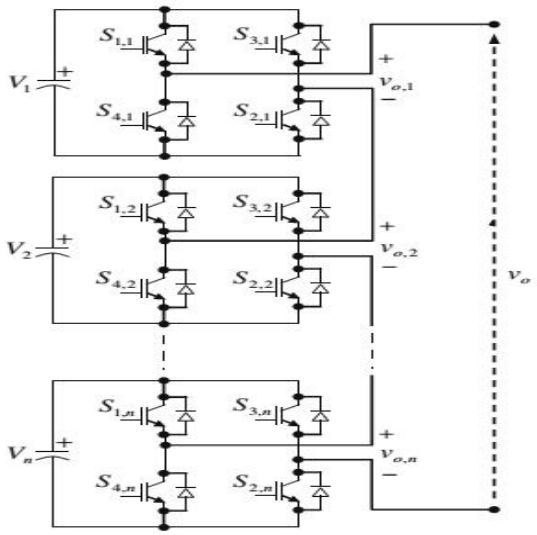

Fig 2.1: Configuration of cascaded multilevel inverter

On the off chance that all dc voltage sources in Fig.2.1 equivalent to Vdc, the inverter is known as symmetric multilevel inverter. The powerful number of yield voltage steps (Nstep) in symmetric multilevel inverter might be identified with the quantity of full-extensions (n) by:

$$N_{step} = 2n+1 \quad (2)$$

And the maximum output voltage ($V_{o,max}$) of this n cascaded multilevel inverter is

$$V_{o,max} = n \times V_{dc} \quad (3)$$

To give an expansive number of output steps without expanding the quantity of inverters, asymmetric multilevel inverters can be utilized. In [11, 12], the dc voltages sources are proposed to be picked by geometric movement with a variable of a few. For n cascaded multilevel inverters, the quantity of voltage steps is given as takes after:

$$N_{step} = (2^{n+1} -1), \text{ if } V_k = 2^{k-1} V_{dc} \text{ for k=1,2,3.....n} \quad (4)$$

$$N_{step} = 3^n \text{ , if } V_k = 3^{k-1} V_{dc} \text{ for k=1,2,3.....n} \quad (5)$$

The maximum output voltages of these n cascaded multilevel inverters are:

$$V_{o,max} = (2^n-1)V_{dc}, \text{ if } V_k = 2^{k-1} V_{dc} \text{ for k=1,2,3.....n} \quad (6)$$

$$V_{o,max} = ((3^n-1)/2)V_{dc}, \text{ if } V_k = 3^{k-1} V_{dc} \text{ for k=1,2,3.....n} \quad (7)$$

Contrasting the Eqs. (2)–(7), it can be seen that the asymmetric multilevel inverters can produce more voltage steps & higher most extreme yield voltage with the same number of bridges.

3. Proposed Level Generator

Fig.3.1 demonstrates the recommended fundamental unit for a sub-multilevel inverter. This comprises of a capacitor (with dc voltage equivalent to Vdc) with one switche S1 and diode D1.

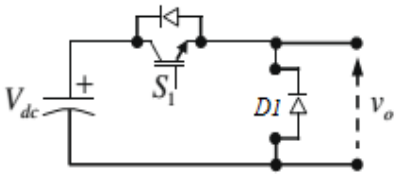

Fig 3.1: Basic Unit for a Sub-Multilevel Converter

Fig.3.2 shows cascaded connecion of proposed submulti level inverter topology.

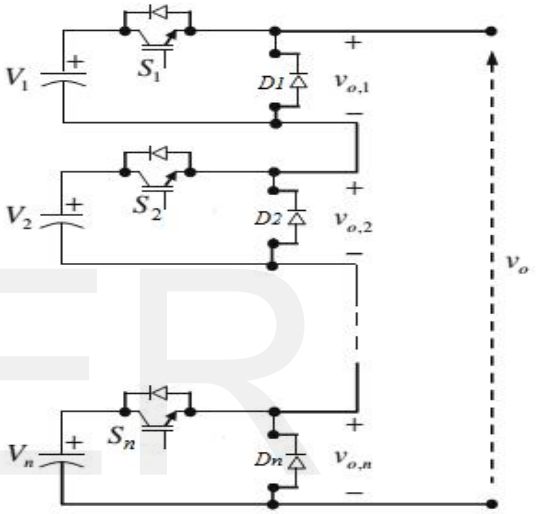

Fig 3.2: Cascaded basic units for level generation

This topology of inverter uses submultilevel inverter part and polarity maker. The submultilevel converter gives either zero or positive .The submultilevel converter canbe worked in three modes given as takes after

3.1 First strategy

On the off chance that all dc voltage sources in Fig. 3.2 equivalent to Vdc, the inverter is then known as symmetric multilevel inverter. The quantity of maximum voltage step of the n arrangement essential units can be assessed by:

$$N_{step} = n+1 \quad (8)$$

The explanation behind utilizing the term "most extreme" is that it is conceivable to have an equivalent worth for Vo over various conditions of the switches. The most extreme yield voltage is given by:

$$V_{o,max} = n \times V_{dc} \quad (9)$$

3.2 Second strategy

The second strategy for assurance of the sizes of dc voltage sources is in binary fashion which gives an exponential expanding in the quantity of the general yield levels. For n arrangement fundamental units, with dc voltage levels fluctuating in binary fashion, the quantity of greatest yield voltage steps and most extreme yield voltage are ascertained by Eqs. (10) and (6), separately.

$$N_{step} = 2^n \quad (10)$$

3.3 Third strategy

In the third strategy, the dc voltage sources in the proposed multilevel inverters are prescribed to be picked by taking after conditions:

$$V_1 = V_{dc} \quad (11)$$

$$V_k = 2V_{dc} \text{ for } k=2, 3, 4...n \quad (12)$$

The quantity of most extreme yield voltage steps can be controlled by the accompanying condition:

$$N_{step} = 2n \quad (13)$$

The most extreme yield voltage of this n cascaded multilevel inverter is:

$$V_{o,max} = (2n-1)V_{dc} \quad (14)$$

4.Proposed Inverter Topology

The multilevel proposed in Fig.3.2, just can create the positive yield voltages. For creating both of the positive and negative yield voltages, the structure appeared in Fig.4.1 is proposed. In this figure, the full-bridge topology added to the yield terminals of the circuit appeared in Fig.3.2. The bearing of burden current and voltage are as appeared in Fig.4.1.Proposed multilevel inverter Fig.4.1 is separated into two principle parts initial one is a level generator for producing required level of yield and second part is polarity maker for creating positive and negative levels at yield.

4.1 Circuit Description

In traditional multilevel inverters, the power semiconductor switches are consolidated to create a high-frequency waveform in positive and negative polarities. Be that as it may, there is no compelling reason to use all the switches for producing bipolar levels. Level generation part is in charge of level creating in positive polarity.

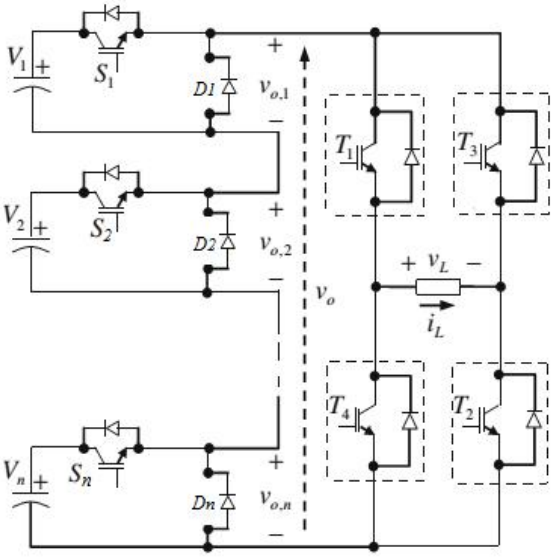

Fig.4.1 Proposed multilevel inverter topology

This part requires high- frequency switches to create the required levels. The switches in this part ought to have high- switching-frequency capability. The other part is called polarity generation part and is in charge of creating the extremity of the yield voltage, which is the low-frequency part working at line frequency. Keeping in mind the end goal to produce a complete multilevel yield, the positive levels are created by the high- frequency part (level era), and after that, this part is sustained to a full-bridge inverter (polarity generation), which will produce the required polarity for the yield. This will wipe out a considerable lot of the semiconductor switches which were capable to create the yield voltage levels in positive and negative polarities

In the topology shown in Fig. 4.1. The quantity of greatest yield voltage levels for three strategies specified in Section 3 are given by the accompanying conditions, separately:

i. First strategy: $N_{level} = 2n + 1$ (15)

ii. Second strategy: $N_{level} = 2^{n+1}-1$ (16)

iii. Third strategy: $N_{level} = 4n - 1$ (17)

Proposed topology is studied by considering cascaded connection of three sub multilevel converters in above mentioned three methods as given as follows.

4.1.1 Operation of proposed inverter in 1st method

In the simulation Vpu= 50V is considered so the value of the three dc sources are 50V, 50V and 50V as per the equation. With the given magnitude of dc voltage source the seven voltage levels are generated by the combination of the switches for the proposed inverter topology shown in Fig.4.1.

TABLE-I
Switching Combination Required To Generate Each Output Voltage Step

Output Voltage	Switching States						
	S_1	S_2	S_3	D_1	D_2	D_3	Steps
0V	0	0	0	1	1	1	1
50V	0	0	1	1	1	0	2
100V	0	1	1	1	0	0	3
150V	1	1	1	0	0	0	4

4.1.2 Operation of proposed inverter in 2nd method

In the simulation Vpu= 25V is considered so the value of the three dc sources are 25V ,50V and 100V as per the equation.With the given magnitude of dc voltage source the Fifteen voltage levels are generated by the combination of the switches for the proposed inverter topology shown in Fig.4.1.

TABLE-II
Switching Combination Required To Generate Each Output Voltage Step

Output Voltage	Switching States						
	S_1	S_2	S_3	D_1	D_2	D_3	Steps
0V	0	0	0	1	1	1	1
25V	0	0	1	1	1	0	2
50V	0	1	0	1	0	1	3
75V	0	1	1	1	0	0	4
100V	1	0	0	0	1	1	5
125V	1	0	1	0	1	0	6
150V	1	1	0	0	0	1	7
175V	1	1	1	0	0	0	8

4.1.3 Operation of proposed inverter in 3rd method

In the simulation Vpu= 25V is considered so the value of the three dc sources are 25V ,50V and 50V as per the equation.With the given magnitude of dc voltage source the Eleven voltage levels are generated by the combination of the switches for the proposed inverter topology shown in Fig.4.1.

TABLE-III
Switching Combination Required To Generate Each Output Voltage Step

Output Voltage	Switching States						
	S_1	S_2	S_3	D_1	D_2	D_3	Steps
0V	0	0	0	1	1	1	1
25V	0	0	1	1	1	0	2
50V	0	1	0	1	0	1	3
75V	0	1	1	1	0	0	4
100V	1	1	0	0	0	1	5
125V	1	1	1	0	0	0	6

4.2 Number of Components Required

One of the vital points of the proposed topology is that it requires less number of high- switching frequency power semiconductor switches. Therefore the dependability of the converter is expanded. It can be clearly seen that the amount of parts of the power stage is lower than that of various topologies like the diode clamped & flying capacitor designs,and a new & exceptionally enhanced multilevel stage. Table IV demonstrates the correlation of number of components required for various Fifteen level inverter topologies[13].

TABLE-IV
Number Of Components Required For Single Phase Fifteen-Level Inverter Topologies

MLI Type	Diode Clamped	Flying Capacitor	CHB	Proposed Topology
Main Switches	28	28	28	7
Diodes	210	28	28	10
Capacitors	14	105	7	3
Total Number	252	161	63	20

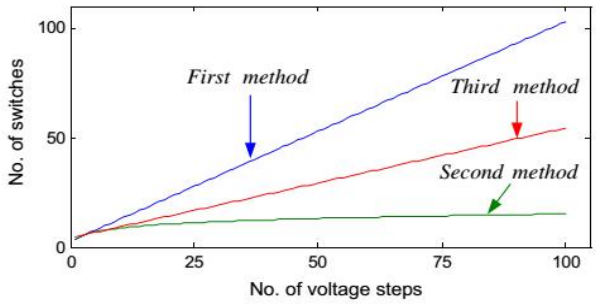

Fig.4.2.Comparison of proposed topology in three methods

In the proposed topology numbers of switches required are less in second method compared to first & third. Fig.4.2 shows comparison of proposed topology in three methods.

5. Multilevel PWM Modulation

The tweak plans for CMLIs are generally taking into account different bearer courses of action with PWM (pulse width modulation).In this way, in the conventional PWM plan, the N voltage levels need N carrier signals that are organized with vertical movements or even relocations. Accordingly, the high-order harmonic components generated by the PWM plan can be weakened effortlessly by filter or load inductance, consequently giving a yield voltage great reference following and low symphonious bending. In any case, it additionally prompts high switching losses as the device switching frequency is usually quite high. In the meantime, N carrier signals make the execution exceptionally complicated. Subsequently, staircase modulation[14] with low device switching frequency is presented. Fig.5.1 demonstrates the stepped-voltage waveform comprising of the yield of the 3-H-bridge modules with switching angles of triggering signals. The switches are switched at very low frequency and the inverter is driven by fundamental switching strategy prompts low electromagneticinterference (EMI). It comprises of eight switching angles(ɵ1 to ɵ 8) at which every level is produced and the switches are switched.

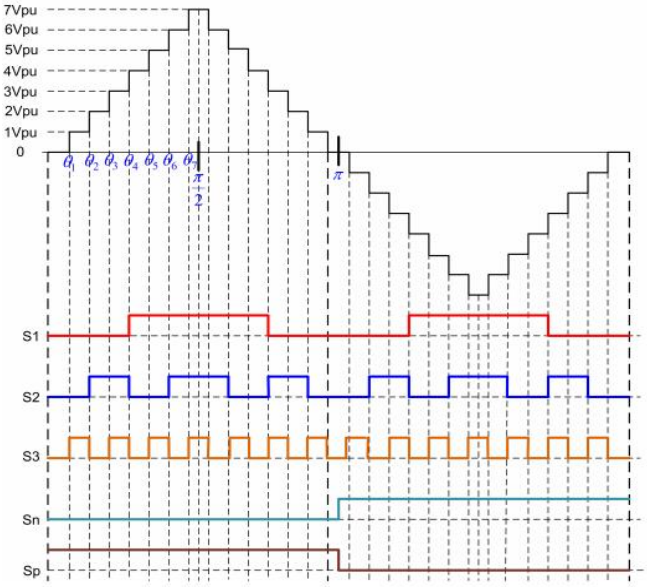

Fig. 5.1: Stepped-voltage waveform consists of switching angles for IGBTs

In this paper sinusoidal wave is taken as reference for staircase modulation for proposed topology.

The reference sine wave is having most extreme amplitude of 1 and is separated into seven stages of equivalent size equivalent to 1/8 = 0.125.Each stage relating to for switching angle for specific switch. The logic functions for the gate signals are generated based on on off sequence of each swich as shown in Fig.5.2.In this paper sine wave as a reference wave by connecting absolute sine wave is taken and from this gating signals are produced and afterward we can trigger the IGBTs.

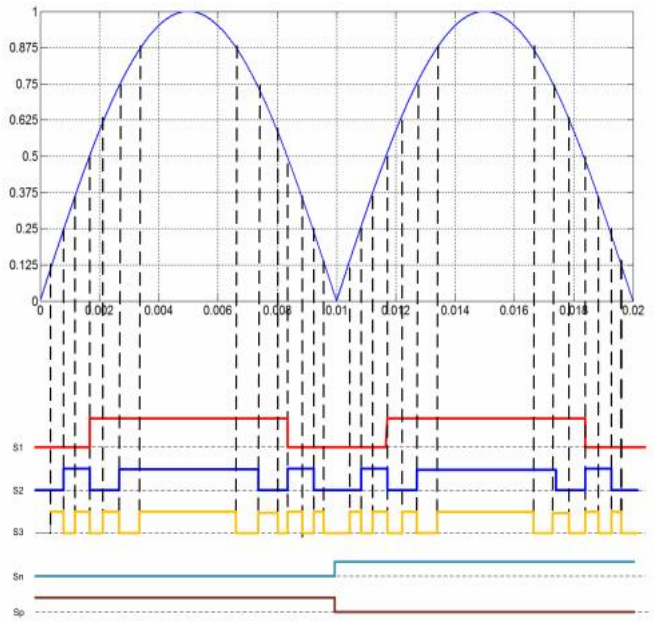

Fig. 5.2: Reference sine wave and gating signals.

The switching frequency of this circuit can be given by:

$$f\_switch = f\_fundamental \times 2(2^n - 1) \quad (18)$$

Where the fundamental frequency is 50Hz, n speaks to the quantity of the specific H-bridge in per unit voltage order. The H-bridge with higher voltage yield works at a lower switching frequency contrasting with the H-bridge with lower voltage yield, which lessens the switching losses mostly. Table V shows switching frequencies of switches of proposed topology in three methods.

TABLE-V
Switching Frequency Comparision

Switches	S_1	S_2	S_3
1st Method (7 level)	100Hz	100Hz	100Hz
2nd Method (15 level)	100Hz	300Hz	700Hz
3rd Method (11 level)	100Hz	100Hz	300Hz

6. Simulation Results

So as to confirm the proposed inverter topology and the switching sequence, simulations are performed by utilizing MATLAB/SIMULINK.

The output of level generator in first, second and third methods is given as follows

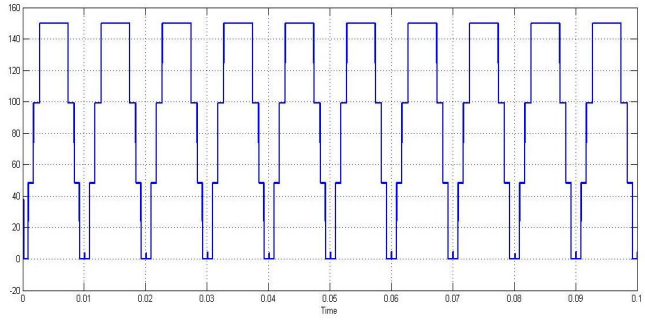

Fig.6.1. Output of level generator in seven level inverter

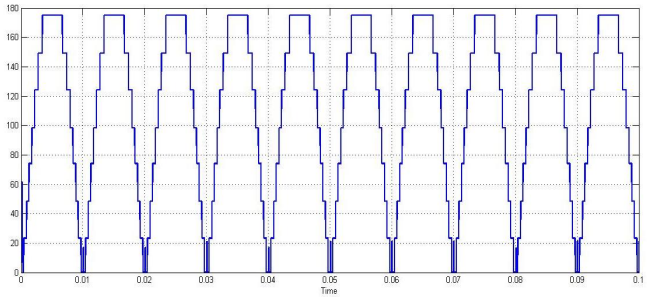

Fig.6.2. Output of level generator in fifteen level inverter

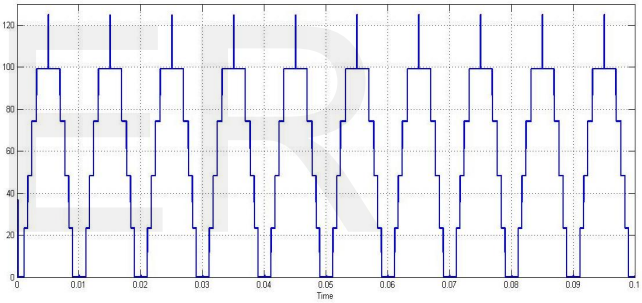

Fig.6.3. Output of level generator in eleven level inverter

The waveforms of the proposed seven level Symmetric (1st method)multilevel inverter with R- Load & a series R-L load of 150Ω & 30mH respectively are shown in Figures.

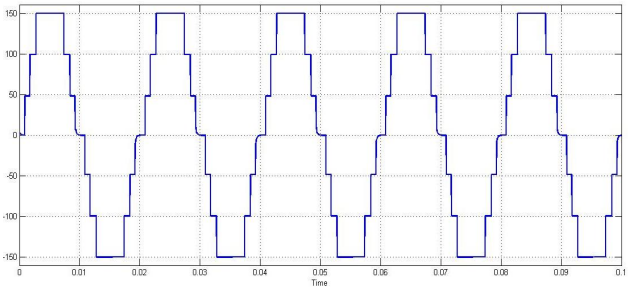

Fig.6.4. Output voltage of Seven level inverter with R(150Ω)Load

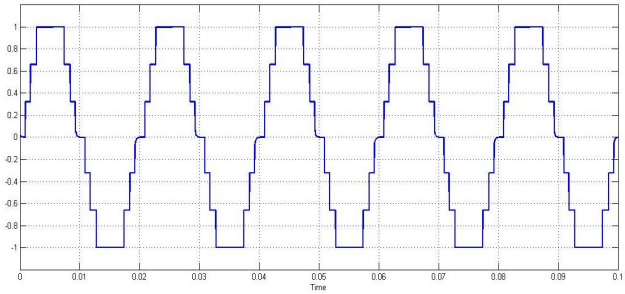

Fig.6.5. Output current of Seven level inverter with R(150Ω)Load

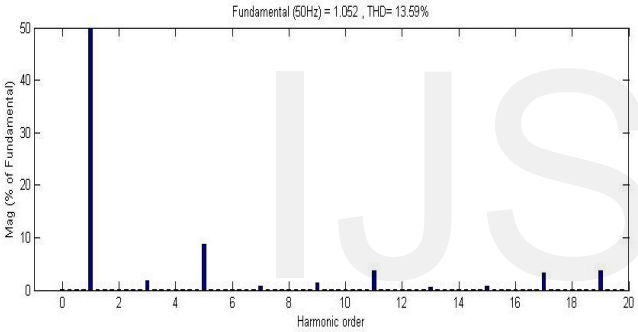

Fig.6.6. Output current THD Seven level inverter with R- Load

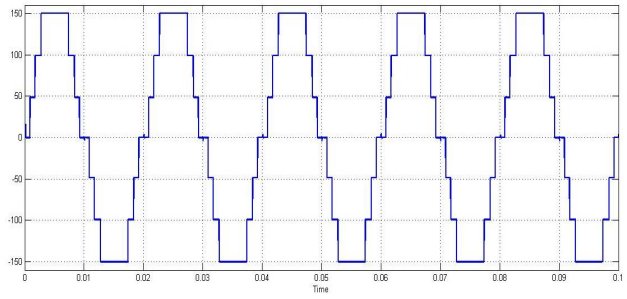

Fig.6.7. Output voltage of Seven level inverter with RL(150 Ω,30mH)-Load

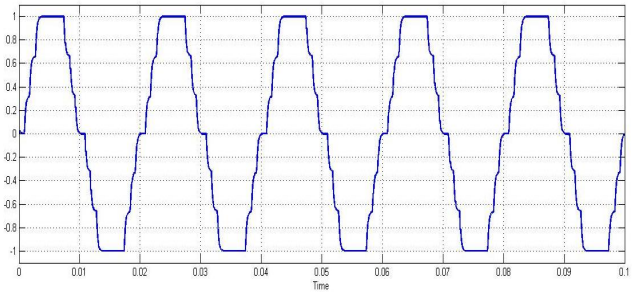

Fig.6.8. Output current of Seven level inverter with RL(150 Ω,30mH)-Load

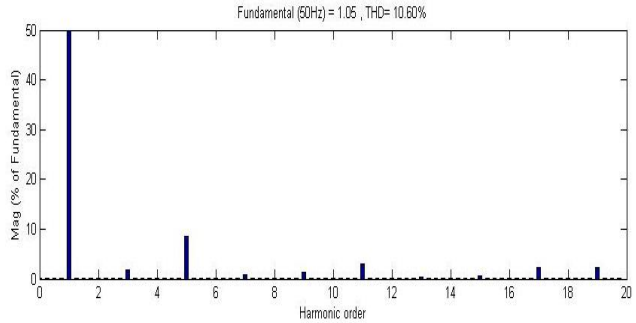

Fig.6.9. Output current THD Seven level inverter with RL- Load

The waveforms of the proposed Fifteen level Asymmetric(2nd method) multilevel inverter with R- Load & a series R-L load of 150Ω & 30mH respectively are shown in Figures.

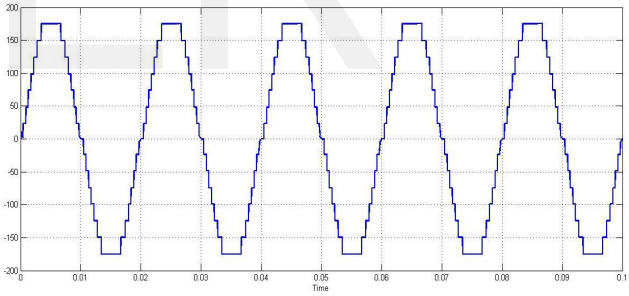

Fig.6.10. Output voltage of Fifteen level inverter with R(150Ω)Load

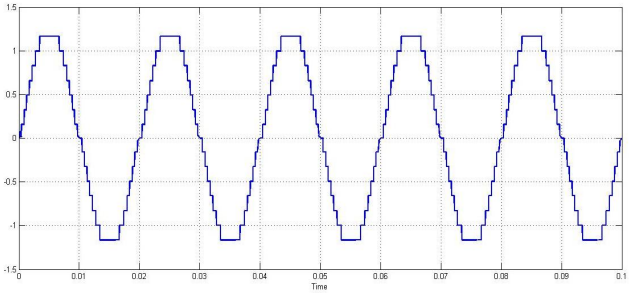

Fig.6.11. Output current of Fifteen level inverter with R(150Ω)Load

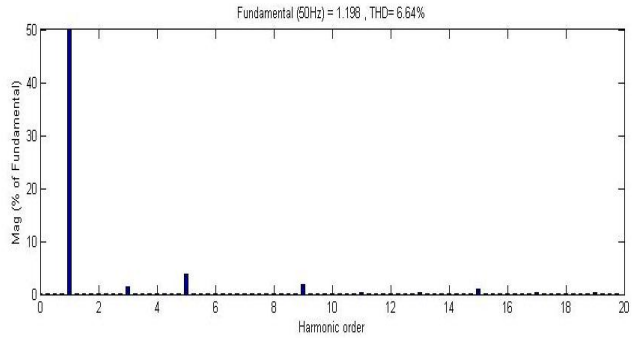

Fig.6.12. Output current THD Fifteen level inverter with R- Load

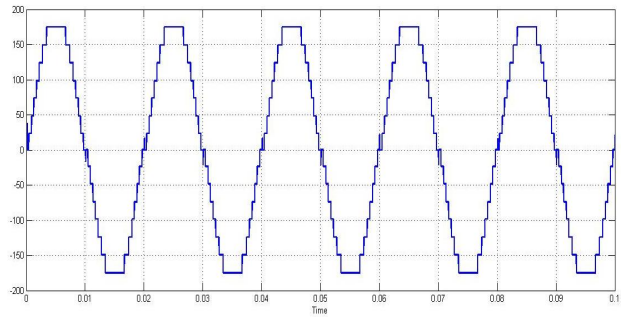

Fig.6.13. Output voltage of Fifteen level inverter with RL(150 Ω,30mH)-Load

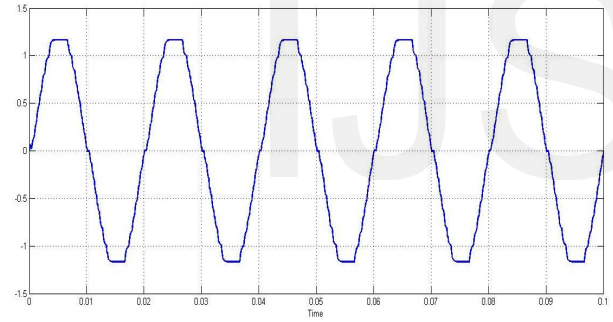

Fig.6.14. Output current of Fifteen level inverter with RL(150 Ω,30mH)-Load

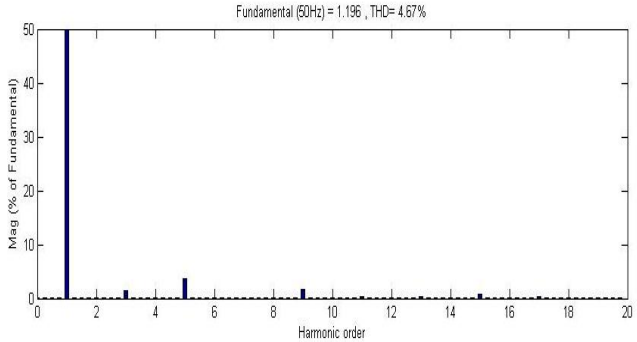

Fig.6.15. Output current THD Fifteen level inverter with RL- Load

Table VI Shows THD comparison of Proposed Topology in Three Methods without any filter at load terminals.

TABLE VI THD Comparison

MLI Type	Voltage THD %		Current THD%	
	R-Load	RL-Load	R-Load	RL-Load
3rd Method (11 Level)	18.15	18.43	18.15	16.30
1st Method (7 Level)	13.59	13.92	13.59	10.60
2nd Method (15 Level)	6.64	6.80	6.64	4.67

7. Conclusion

In this paper studied an inverter topology which has improved performance, offering superior output waveforms and lower THD over conventional topology in terms of number of switches required, cost, control system and reliability. The number of power semiconductor switches required for the proposed inverter is very less in number also the switching frequencies are less compared to other pwm techniques and these reduces switching losses largely. Proposed topology is studied for three different levels of output voltages 7, 11 & 15 respectively with Resistive and Inductive loads. Obtained results are satisfactory with reduced THD content in the output and also the complexity of switching for this topology is low. The results obtained clearly shows the effectiveness of the proposed topology as an asymmetric fifteen level inverter compared to symmetric 7 & 11 level with reduced number of switches & reduced THD. This proposed multilevel inverter Topology can be extended for higher number of levels with few number of changes made in proposed topology.

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